Notice of Allowability	Application No.	Applicant(s)	
	10/760,429	HEISHI ET AL.	
	Examiner	Art Unit	
	Qing Chen	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on November 26, 2007*.

2. ☒ The allowed claim(s) is/are *60-72, renumbered as 1-13*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This Office action is in response to the amendment filed on November 26, 2007.

2. **Claims 60-72** are pending.

3. **Claims 60-72** have been amended.

4. **Claims 1-59** have been cancelled.

5. **Claims 60-72** are allowed, renumbered as 1-13.

6. The objection to the title is withdrawn in view of Examiner's amendments to the title.

7. The objection to the abstract is withdrawn in view of Applicant's amendments to the abstract.

8. The 35 U.S.C. § 112, second paragraph, rejections of Claims 2-8, 11, 12, 14, 22-26, 28, 29, 32, 34, 39, 40, 43, 44, 47, 49, and 54-56 are withdrawn in view of Applicant's cancellation of the claims.

9. The 35 U.S.C. § 101 rejections of Claims 1-26 and 42-59 are withdrawn in view of Applicant's cancellation of the claims.

Examiner's Amendment

10. An Examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to Applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this Examiner's amendment was given in a telephone interview with Andrew L. Dunlap (Reg. No. 60,554) on February 5, 2008.

The application has been amended as follows:

AMENDMENT TO THE TITLE OF THE INVENTION

Please replace the original title of the invention with the following rewritten title.

COMPILER APPARATUS AND METHOD ~~FOR~~ OF OPTIMIZING A SOURCE PROGRAM BY REDUCING A HAMMING DISTANCE BETWEEN TWO INSTRUCTIONS

In the Claims:

Please amend Claims 60-72 as follows:

AMENDMENTS TO THE CLAIMS

Claims 1-59 (Cancelled)

Claim 60 (Currently Amended) A computer-readable storage medium encoded with a compiler apparatus for generating a machine language program for a processor, the processor including a plurality of instruction issue units and a plurality of corresponding execution units, each instruction issue unit issuing instructions to a corresponding execution unit, and each instruction issue unit including instruction registers for storing the instructions issued to the corresponding execution unit, the compiler apparatus comprising:

a parser unit operable to parse ~~the~~ a source program by extracting, from the source program, a reserved word stored in a storage unit and by carrying out a lexical analysis of the source program;

an intermediate code conversion unit operable to receive the parsed source program and convert each statement included in the parsed source program into intermediate codes according to a predetermined rule stored in the storage unit, the intermediate codes including instructions;

an optimization unit operable to receive the intermediate codes and optimize scheduling of the instructions of the intermediate codes by:

scheduling the instructions of the intermediate codes for each instruction cycle of a plurality of instruction cycles without changing dependencies between the instructions of the intermediate codes, each of the instruction cycles being an instruction cycle that executes instructions in parallel using the execution units; and

scheduling the instructions of the intermediate codes to reduce a hamming distance between two instructions including (i) an instruction in a target instruction cycle, and (ii) an instruction in an instruction cycle that immediately precedes the target instruction cycle, the two instructions being instructions stored in instruction registers of the same instruction issue unit, the optimization unit being operable to schedule the instructions of the intermediate codes to reduce the hamming distance of instructions which are scheduled for each of the instruction cycles; and

a code generation unit operable to receive the optimized intermediate codes and convert the optimized intermediate codes into machine language instructions according to a conversion table stored in the storage unit.

Claim 61 (Currently Amended) The computer-readable ~~recording~~ storage medium according to claim 60, wherein the optimization unit is operable to optimize the instructions of the intermediate codes by determining an instruction to be executed in the target instruction cycle and determining an instruction issue unit in which the instruction is to be stored so as to reduce a hamming distance between the two instructions when the instructions of the intermediate codes are scheduled for each of the instruction cycles.

Claim 62 (Currently Amended) The computer-readable ~~recording~~ storage medium according to claim 61, wherein the optimization unit is operable to optimize the instructions of the intermediate codes by determining which instruction is to be executed in the target instruction cycle and determining which instruction register of the instruction issue unit storing the instruction is for storing the instruction, to reduce the hamming distance between the two instructions when the instructions of the intermediate codes are scheduled for each of the instruction cycles.

Claim 63 (Currently Amended) The computer-readable ~~recording~~ storage medium according to claim 60, wherein the optimization unit is operable to optimize the instructions of the intermediate codes by scheduling the instructions of the intermediate codes to reduce a hamming distance between operation codes of the two instructions, the two instructions being stored in instruction registers of the same instruction issue unit.

Claim 64 (Currently Amended) The computer-readable ~~recording~~ storage medium according to claim 60, wherein the optimization unit is operable to optimize the instructions of the intermediate codes by scheduling the instructions of the intermediate codes to reduce a hamming distance between register numbers of the two instructions when the instructions of the intermediate codes are scheduled for each of the instruction

cycles, the two instructions being stored in instruction registers of the same instruction issue unit.

Claims 65 (Currently Amended) A computer-readable storage medium encoded with a compiler apparatus for generating a machine language program for a processor, the processor including a plurality of instruction issue units and a plurality of corresponding execution units, and each instruction issue unit issuing instructions to a corresponding execution unit, and each instruction issue unit including instruction registers for storing the instructions issued to the corresponding execution unit, the compiler apparatus comprising:

a parser unit operable to parse ~~the~~ a source program by extracting, from the source program, a reserved word stored in a storage unit and by carrying out a lexical analysis of the source program;

an intermediate code conversion unit operable to receive the parsed source program and convert each statement included in the parsed source program into intermediate codes according to a predetermined rule stored in the storage unit, the intermediate codes including instructions;

an optimization unit operable to receive the intermediate codes and optimize the instructions of the intermediate codes by:

changing, for each instruction cycle of a plurality of instruction cycles, a correspondence between (i) instructions of the intermediate codes to be executed in the same instruction cycle and (ii) the instruction issue units from which the instructions are issued, the optimization unit changing the correspondence without changing dependencies between the instructions of the intermediate codes converted by the intermediate code conversion unit, and each of the instruction cycles being an instruction cycle that executes instructions in parallel using the execution unit; and

changing the correspondence between (i) instructions to be executed in a target instruction cycle and (ii) the instruction issue units from which the instructions are issued, to reduce a hamming distance between two instructions including an instruction to be executed in the target instruction cycle and an instruction in an instruction cycle that

immediately precedes the target instruction cycle, the two instructions being instructions stored in instruction registers of the same instruction issue unit; and

a code generation unit operable to receive the optimized intermediate codes and convert the optimized intermediate codes into machine language instructions according to a conversion table stored in the storage unit.

Claim 66 (Currently Amended) The computer-readable ~~recording~~ storage medium according to claim 65, wherein the optimization unit is operable to optimize the instructions of the intermediate codes by changing the correspondence between (i) the instructions to be executed in the target instruction cycle, and (ii) the instruction issue units from which the instructions are issued, to reduce a sum of hamming distances, each of the hamming distances being calculated between the two instructions, the two instructions being issued to an identical instruction issue unit, and the two instructions used to calculate the sum of the hamming distances being included in the instruction issue units, respectively.

Claim 67 (Currently Amended) The computer-readable ~~recording~~ storage medium according to claim 65, wherein the optimization unit is operable to optimize the instructions of the intermediate codes by changing the correspondence between (i) the instructions to be executed in the target instruction cycle, and (ii) the instruction issue units in which the instructions are issued, to reduce a hamming distance between operation codes of the two instructions.

Claim 68 (Currently Amended) The computer-readable ~~recording~~ storage medium according to claim 65, wherein the optimization unit is operable to optimize the instructions of the intermediate codes by changing the correspondence between (i) the instructions to be executed in the target instruction cycle, and (ii) the instruction issue units in which the instructions are issued, to reduce a hamming distance between register numbers of the two instructions.

Claim 69 (Currently Amended) A method for generating a machine language program for a processor, the processor including a plurality of instruction issue units and a plurality of corresponding execution units, each instruction issue unit issuing instructions to a corresponding execution unit, and each instruction issue unit including instruction registers for storing the instructions issued to the corresponding execution unit, the method comprising:

parsing ~~the~~ a source program by extracting, from the source program, a reserved word stored in a storage unit and by carrying out a lexical analysis of the source program;

converting each statement included in the parsed source program into intermediate codes according to a predetermined rule stored in the storage unit, the intermediate codes including instructions;

optimizing scheduling of the instructions of the intermediate codes by:

scheduling the instructions of the intermediate codes for each instruction cycle of a plurality of instruction cycles without changing dependencies between the instructions of the intermediate codes, each of the instruction cycles being an instruction cycle that executes instructions in parallel using the execution units; and

scheduling the instructions of the intermediate codes to reduce a hamming distance between two instructions including (i) an instruction in a target instruction cycle, and (ii) an instruction in an instruction cycle that immediately precedes the target instruction cycle, the two instructions being instructions stored in instruction registers of the same instruction issue unit, and the scheduling of the instructions of the intermediate codes reducing the hamming distance of instructions scheduled for each of the instruction cycles; and

converting the optimized intermediate codes into machine language instructions according to a conversion table stored in the storage unit.

Claim 70 (Currently Amended) A method for generating a machine language program for a processor, the processor including a plurality of instruction issue units and a plurality of corresponding execution units, each instruction issue unit issuing instructions to a corresponding execution unit, and each instruction issue unit including

instruction registers for storing the instructions issued to the corresponding execution unit, the method comprising:

parsing ~~the~~ a source program by extracting, from the source program, a reserved word stored in a storage unit and by carrying out a lexical analysis of the source program;

converting each statement included in the parsed source program into intermediate codes according to a predetermined rule stored in the storage unit, the intermediate codes including instructions;

optimizing the instructions of the intermediate codes by:

changing, for each instruction cycle of a plurality of instruction cycles, a correspondence between (i) instructions of the intermediate codes to be executed in the same instruction cycle and (ii) the instruction issue units from which the instructions are issued, the optimization unit changing the correspondence without changing dependencies between the instructions of the intermediate codes converted by the converting of each statement, and each of the instruction cycles being an instruction cycle that executes instructions in parallel using the execution units; and

changing the correspondence between (i) instructions to be executed in a target instruction cycle and (ii) the instruction issue units from which the instructions are issued, to reduce a hamming distance between two instructions including an instruction to be executed in the target instruction cycle and an instruction in an instruction cycle that immediately precedes the target instruction cycle, the two instructions being instructions stored in instruction registers of the same instruction issue unit; and

converting the optimized intermediate codes into machine language instructions according to a conversion table stored in the storage unit.

Claim 71 (Currently Amended) A computer-readable storage medium encoded with a compiler program for generating a machine language program for a processor, the processor including a plurality of instruction issue units and a plurality of corresponding execution units, each instruction issue unit issuing instructions to a corresponding execution unit, and each instruction issue unit including instruction registers for storing the instructions issued to the corresponding execution unit, the compiler program causing a computer to execute a method comprising:

parsing ~~the~~ a source program by extracting, from the source program, a reserved word stored in a storage unit and by carrying out a lexical analysis of the source program;

converting each statement included in the parsed source program into intermediate codes according to a predetermined rule stored in the storage unit, the intermediate codes including instructions;

optimizing scheduling of the instructions of the intermediate codes by:

scheduling the instructions of the intermediate codes for each instruction cycle of a plurality of instruction cycles without changing dependencies between the instructions of the intermediate codes, each of the instruction cycles being an instruction cycle that executes instructions in parallel using the execution units; and

scheduling the instructions of the intermediate codes to reduce a hamming distance between two instructions including (i) an instruction in a target instruction cycle, and (ii) an instruction in an instruction cycle that immediately precedes the target instruction cycle, the two instructions being instructions stored in instruction registers of the same instruction issue unit, the scheduling of the instructions of the intermediate codes reducing the hamming distance of instructions scheduled for each of the instruction cycles; and

converting the optimized intermediate codes into machine language instructions according to a conversion table stored in the storage unit.

Claim 72 (Currently Amended) A computer-readable storage medium encoded with a compiler program for generating a machine language program for a processor, the processor including a plurality of instruction issue units and a plurality of corresponding execution units, each instruction issue unit issuing instructions to a corresponding execution unit, and each instruction issue unit including instruction registers for storing the instructions issued to the corresponding execution unit, the compiler program causing a computer to execute a method comprising:

parsing ~~the~~ a source program by extracting, from the source program, a reserved word stored in a storage unit and by carrying out a lexical analysis of the source program;

converting each statement included in the parsed source program into intermediate codes according to a predetermined rule stored in the storage unit, the intermediate codes including instructions;

optimizing the instructions of the intermediate codes by:

changing, for each instruction cycle of a plurality of instruction cycles, a correspondence between (i) instructions of the intermediate codes to be executed in the same instruction cycle and (ii) the instruction issue units from which the instructions are issued, the optimization unit changing the correspondence without changing dependencies between the instructions of the intermediate codes converted by the converting of each statement, and each of the instruction cycles being an instruction cycle that executes instructions in parallel using the execution units; and

changing the correspondence between (i) instructions to be executed in a target instruction cycle and (ii) the instruction issue units from which the instructions are issued, to reduce a hamming distance between two instructions including an instruction to be executed in the target instruction cycle and an instruction in an instruction cycle that immediately precedes the target instruction cycle, the two instructions being instructions stored in instruction registers of the same instruction issue unit; and

converting the optimized intermediate codes into machine language instructions according to a conversion table stored in the storage unit.

-- END OF AMENDMENT --

Reasons for Allowance

11. The following is an Examiner's statement of reasons for allowance:

The cited prior art taken alone or in combination fail to teach, in combination with the other claimed limitations, "scheduling the instructions of the intermediate codes for each instruction cycle of a plurality of instruction cycles without changing dependencies between the instructions of the intermediate codes, each of the instruction cycles being an instruction cycle that executes instructions in parallel using the execution units; and scheduling the instructions of the intermediate codes to reduce a hamming distance between two instructions including (i) an instruction in a target instruction cycle, and (ii) an instruction in an instruction cycle that immediately precedes the target instruction cycle, the two instructions being instructions stored in instruction registers of the same instruction issue unit, the optimization unit being operable to schedule the instructions of the intermediate codes to reduce the hamming distance of instructions which are scheduled for each of the instruction cycles" as recited in independent Claims 60, 69, and 71; and further fail to teach, in combination with the other claimed limitations, "changing, for each instruction cycle of a plurality of instruction cycles, a correspondence between (i) instructions of the intermediate codes to be executed in the same instruction cycle and (ii) the instruction issue units from which the instructions are issued, the optimization unit changing the correspondence without changing dependencies between the instructions of the intermediate codes converted by the intermediate code conversion unit, and each of the instruction cycles being an instruction cycle that executes instructions in parallel using the execution unit; and changing the correspondence between (i) instructions to be executed in a target instruction cycle and (ii) the instruction issue units from which the

instructions are issued, to reduce a hamming distance between two instructions including an instruction to be executed in the target instruction cycle and an instruction in an instruction cycle that immediately precedes the target instruction cycle, the two instructions being instructions stored in instruction registers of the same instruction issue unit" as recited in independent Claims 65, 70, and 72.

The closest cited prior art, US 5,790,874 (hereinafter "Takano"), teaches an information apparatus permitting a reduction in power consumption according to applications which are being executed by reduce Hamming distances between bit sequences appearing on the instruction bus when the instructions are transferred from the program memory to the processing unit. However, Takano fails to teach "scheduling the instructions of the intermediate codes for each instruction cycle of a plurality of instruction cycles without changing dependencies between the instructions of the intermediate codes, each of the instruction cycles being an instruction cycle that executes instructions in parallel using the execution units; and scheduling the instructions of the intermediate codes to reduce a hamming distance between two instructions including (i) an instruction in a target instruction cycle, and (ii) an instruction in an instruction cycle that immediately precedes the target instruction cycle, the two instructions being instructions stored in instruction registers of the same instruction issue unit, the optimization unit being operable to schedule the instructions of the intermediate codes to reduce the hamming distance of instructions which are scheduled for each of the instruction cycles" as recited in independent Claims 60, 69, and 71; and further fails to teach "changing, for each instruction cycle of a plurality of instruction cycles, a correspondence between (i) instructions of the intermediate codes to be executed in the same instruction cycle and (ii) the instruction issue units from which

the instructions are issued, the optimization unit changing the correspondence without changing dependencies between the instructions of the intermediate codes converted by the intermediate code conversion unit, and each of the instruction cycles being an instruction cycle that executes instructions in parallel using the execution unit; and changing the correspondence between (i) instructions to be executed in a target instruction cycle and (ii) the instruction issue units from which the instructions are issued, to reduce a hamming distance between two instructions including an instruction to be executed in the target instruction cycle and an instruction in an instruction cycle that immediately precedes the target instruction cycle, the two instructions being instructions stored in instruction registers of the same instruction issue unit" as recited in independent Claims 65, 70, and 72.

Any comments considered necessary by Applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Qing Chen whose telephone number is 571-270-1071. The

Examiner can normally be reached on Monday through Thursday from 7:30 AM to 4:00 PM. The Examiner can also be reached on alternate Fridays.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Wei Zhen, can be reached on 571-272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QC
February 11, 2008

WEI ZHEN
SPE TC 2100